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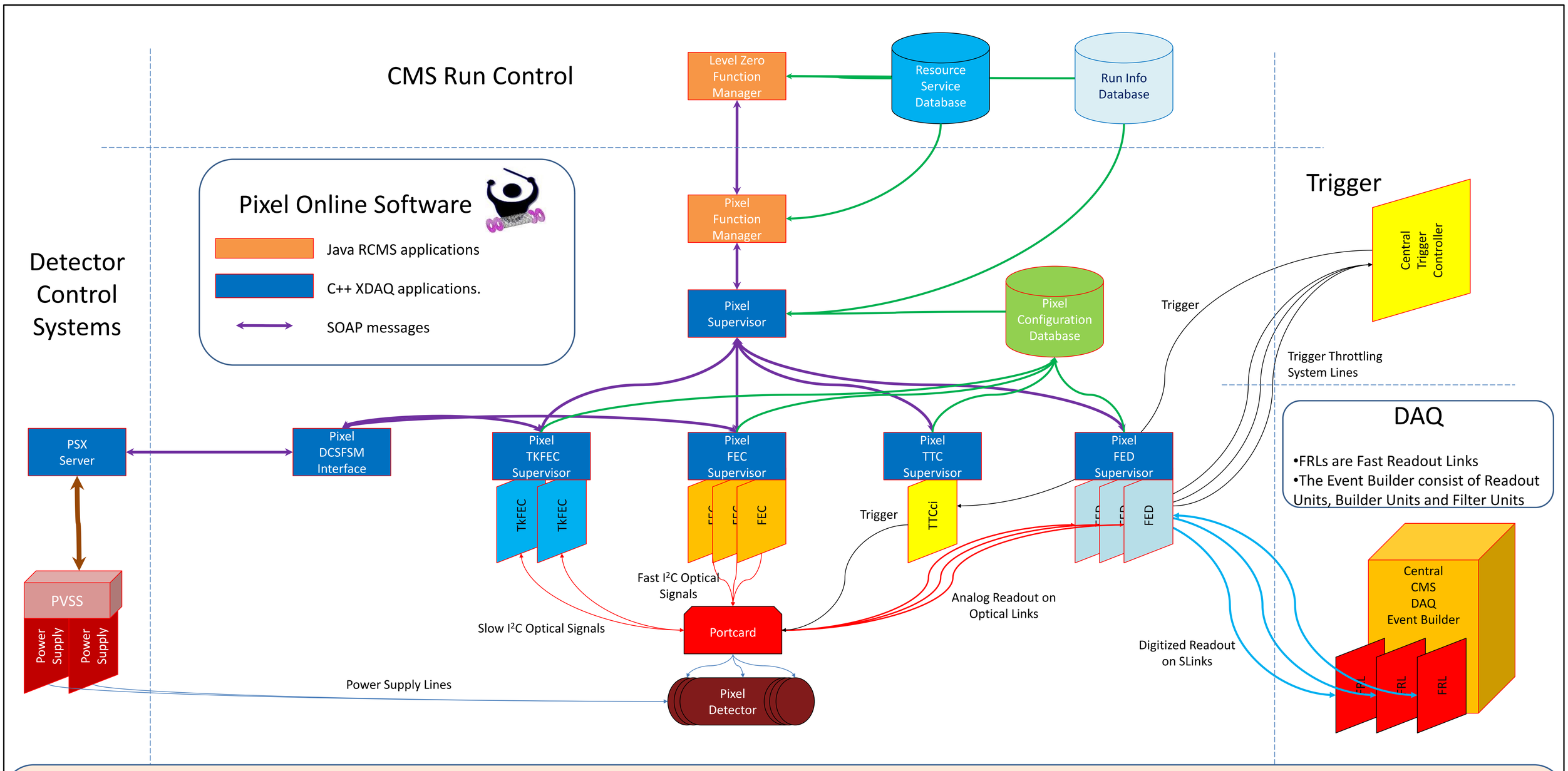
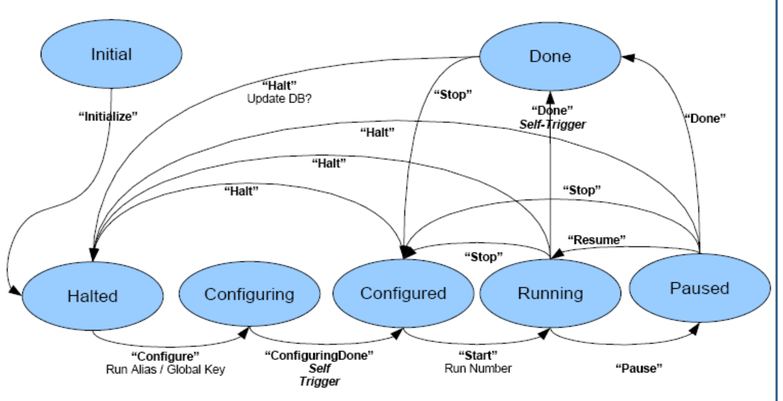
CMS PIXEL ONLINE SOFTWARE

ABSTRACT: The CMS experiment at the LHC incorporates a 66 million channel silicon pixel detector at its center for track seeding and precise vertexing. The Pixel Online Software orchestrates the operation, calibration and monitoring of the pixel detector. It is based on two libraries: XDAQ, a Cross-platform Data Acquisition library written in C++, and RCMS, a Run Control and Monitoring System library written in Java. Applications that comprise Pixel Online Software may be controlled by a pixel detector expert over the world wide web, or by CMS central run control. The various calibrations required to prepare the detector for taking data are carried out using Pixel Online Software. Some characteristics of the readout can also be monitored in real time by the Pixel Online Software. The interaction of the Software with the Detector Control System is used to automatically turn the detector on in stages.



- ➢XDAQ applications communicate with VME boards housed in crates in the counting room. These boards send commands and receive readout from the front-end electronics on the pixel detector.
- ➢Front End Controller (FEC) boards are used to control and program the pixel readout chips. *PixelFECSupervisor* supervises a crate of FEC boards.
- ➢Tracker Front End Controller (TKFEC) boards program the Communications and Control Unit to get the timing right for the Fast I2C signals. *PixelTKFECSupervisor* supervises one TKFEC board.
- ➢Front End Driver (FED) boards receive and digitize analog data from the readout chips. *PixelFEDSupervisor* supervises a crate of FED boards.
- ➢Timing and Trigger Control CMS Interface (TTCci) boards generate trigger patterns or relay them from the Central Trigger Controller (CTC). *PixelTTCSupervisor* supervises one TTCci.
- ➢*PixelSupervisor* orchestrates the aforementioned Supervisors for calibrating the detector and taking data with it. It may be run independently or by run control through *PixelFunctionManager*.

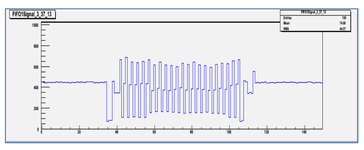
The Finite State Machine Structure



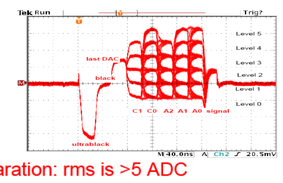
- ➢All the XDAQ supervisors work within a finite state machine framework whose states closely resemble those of Level 0 Function Manager.
- ➢This ensures that the system is in a well defined state at any point in time.
- ➢The inputs for changing the state of *PixelSupervisor*, trickle down to the lower supervisors. But it is not until the states of the lower supervisors have been updated that the state of *PixelSupervisor* can be updated.
- ➢Each lower supervisor can be cycled through its states independently through its own web-based GUI for debugging programming, triggering or readout pathways.
- ➢All calibrations and forms of data taking are implemented within this finite state machine framework.

Some Calibrations

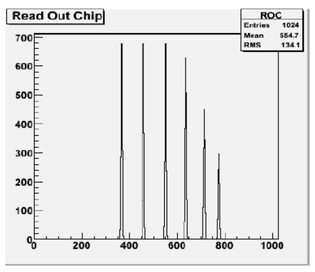
The **FED Baseline Calibration** nearly centers the baseline of all the analog readout lines for the signal to exploit the full dynamical range.



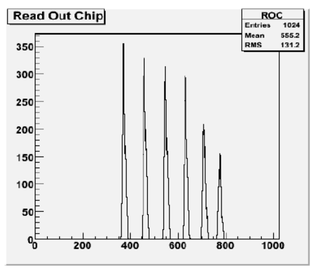
For the FED to decode the analog readout, it must know the address level thresholds. These are determined through **Address Levels Calibration**.



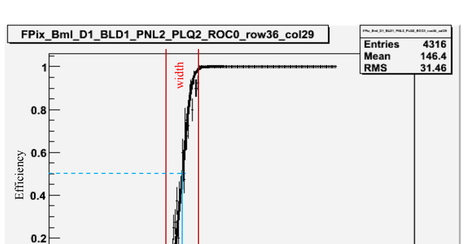
Good separation: rms is ~2.5 ADC



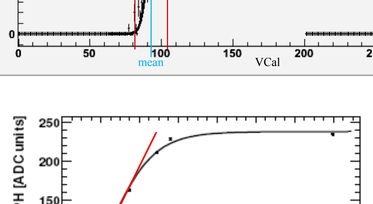
Poor separation: rms is >5 ADC



The *noise* and *threshold* of every pixel is measured by injecting various amounts of charge and plotting the response efficiency in a procedure called the **S-Curve Calibration.**

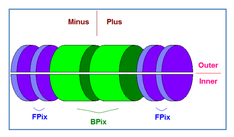


The linearity of response between the amount of charge injected and the pulse height reported is quantified by the **Gain Calibration**.

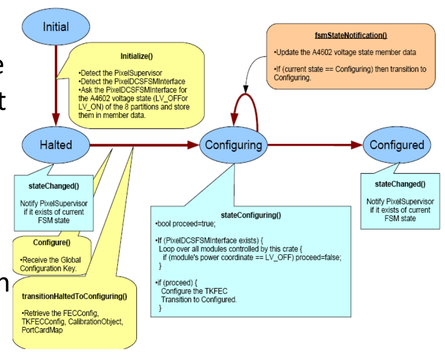


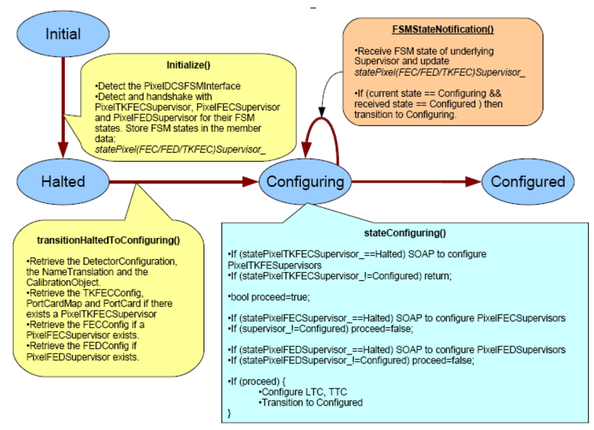
DAQ DCS Integration

For purposes of automatic detector turn-on, the detector is partitioned into 8 segments.



The Portcard and CCUs in the service cylinders have two voltage states: OFF at 0 V and ON at 2.6 V. The *PixelTKFECSupervisor* coordinates with *PixelDCSFSMInterface* to ensure they are turned on before programming.





The readout chips have two voltages of interest, the analog voltage (Vana) and the digital voltage (Vdigi). The Vana can be either OFF (0 V) or ON (1.6 V). The Vdigi for the BPix can be either OFF (0 V) or ON (2.6 V). The Vdigi for the FPix can be either OFF (0 V), ON_REDUCED (2.1 V) or ON (2.6 V). *PixelFECSupervisor* coordinates with *PixelDCSFSMInterface* before programming them.

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