## Pixel Run Control and Calibration

-Souvik Das under Anders Ryd and Karl Ecklund

## The ROC # Mystery and Channel Offset Calibration

- Using the current versions of PixelFEDInterface and PixelFEDSupervisor, we configured the Vanderbilt FED with "params\_fed.dat" with all "Offset DAC Channel"s set to 0.
- The control and mode registers on the FED were set so as to use test-DAC data.
- The test-DAC was programmed with a pulse train corresponding to one ROC header followed by a single pixel hit.
- A VME trigger was generated.
- The Spy FIFO 1 data read out in transparent and normal modes revealed that some of the channels were counting ROC #s starting with 2 instead of 1. *It would be good to understand why the FPGA in the FED can label hits as coming from ROC#2 when the test DAC only has a TBM header and one ROC with one pixel hit.*

## The ROC # Mystery and Channel Offset Calibration



- We plotted the ADC (y-axis) versus test-DAC (x-axis) graph, which was a straight line for all channels and saw that they all had approximately the same slope, but different intercepts. Slope ~ 1.076 and intercept varies from -96.9 to -136.4 depending on channel.
- By changing the "Offset DAC Channel" in "params\_fed.dat" we could shift this intercept. An increase of 1 in the Offset DAC Channel field corresponds roughly to a decrease of 2 in this intercept.
- An ADC-intercept less than -130 seemed to ensure that ROC #s started with 1 instead of 2.
- A Channel Offset Calibration method was implemented in PixelFEDSupervisor to take care of this.
- We might want to look at how the ROC Toggle bit in the transparent mode behaves with changes to the Channel Offset DAC.

## **Address Level Calibration**

- A method of Address Level Calibration is implemented within PixelFEDSupervisor.
- It uses the test-DAC as of now. Pixel hits are simulated on the test-DAC (according to a given human readable .hit file) and then statistics for each level are collected by reading out through spy-FIFO 1.
- The width of each peak comes solely from the noise in the FED between the test-DAC and the ADC output. (No additional Gaussian smearing was done.)
- The threshold levels in "params\_fed.dat" are adjusted accordingly.

• While working on SiDet's (Vanderbilt) FED, some of the channels seemed to be malfunctioning. The last byte of each word in Spy FIFO 1 should be 0x00 if no pixel hit is detected, however, they were 0xff. The only functioning channels were 5, 10, 19, 23, 28, 32 . We hadn't seen this problem when the FED was at Vanderbilt. What's going on here?

